

# High volume production of singlemode VCSELs

Dieter Wiedenmann\*, Martin Grabherr, Roland Jäger, Roger King  
U-L-M photonics GmbH, Albert-Einstein-Allee 45, 89081 Ulm, Germany

## ABSTRACT

Up to now applications for singlemode VCSELs were in low volume and high priced applications like tunable diode laser absorption spectroscopy (TDLAS, [1,2]) or optical interferometers. Typical volumes for these applications are in the range of thousands of pcs per year, with pricing levels of several 100 USD/pcs. New applications for singlemode VCSELs in consumer markets require manufacturing in very high volumes and at very low cost. Examples are laser-based optical mouse sensors, optical encoders, and rubidium atomic clocks for GPS systems [3,4]. U-L-M photonics presents manufacturing aspects, device performance and reliability data for these devices.

The first part of the paper is dealing with high volume manufacturing of 850 nm singlemode VCSEL chips with very high efficiency and low operation current. Special processing technologies have been developed to achieve yields on 3 inch wafers of more than 90 %. Wafer qualification procedures are discussed as well.

The second part of the paper covers high volume packaging in TO and SMT type packages where very high packaging yields must be achieved. In the last part of the paper reliability issues are discussed, focused on the very high susceptibility of these devices to electrostatic discharge.

Keywords: VCSEL, singlemode, sensor, reliability, fabrication

## INTRODUCTION

Following the multi-mode oxide confined VCSEL that made its way into high volume applications mainly in the datacom market of single channel gigabit transceivers, singlemode VCSELs are currently in the transition from a product in niche applications like optical spectroscopy in industrial applications to applications in high volume consumer products. Looking at devices with current confinement and isolation by proton implantation the manufacturability of singlemode devices does not differ considerably from multimode devices. A much more challenging task is the production of singlemode oxide confined devices. These devices are under investigation since more than 10 years [5], [6], [7]. Due to the advantageous current confinement by wet thermal oxidation electro-optical characteristics of these devices are most attractive for applications that require close to ideal laser sources with minimized power dissipation. Having the disadvantage of a relatively high effective index step incorporated into the optical cavity which is unavoidable in oxide confined VCSELs results in only small active diameters that allow for singlemode operation. Active diameters of only 3  $\mu\text{m}$  are challenging to manufacture with high yields due to the very low tolerance in aperture diameter, which must be controlled within  $\pm 0.25 \mu\text{m}$ . Another challenge is the very high sensitivity to electrostatic discharge (ESD) of these devices which demands for an extremely well controlled production environment.

## EPITAXY AND PROCESSING

High volume production of singlemode VCSELs requires both, reproducible supply of epitaxial wafers and superior control of unique semiconductor processing technology. At U-L-M photonics, the epitaxial wafers are grown by solid source MBE on 3-inch substrates in a Riber 49 reactor. The reactor is capable of growing five 3-inch wafers in parallel. Special geometries of wafer holders and effusion cells in the RIBER 49 system result in good homogeneity of the cavity resonance across the 3 inch VCSEL wafers. Figure 1 is giving an example on the wavelength variation obtained with above mentioned technology. In azimuthal direction, the homogeneity of the resonance dip is extremely good and values stay within a  $\pm 0.5 \text{ nm}$  range ( $\pm 0.06 \%$ ). In radial direction, variation is slightly increased and taking edge exclusion area not into account, wavelength variation amounts to  $\pm 1.5 \text{ nm}$  ( $\pm 0.2 \%$ ).

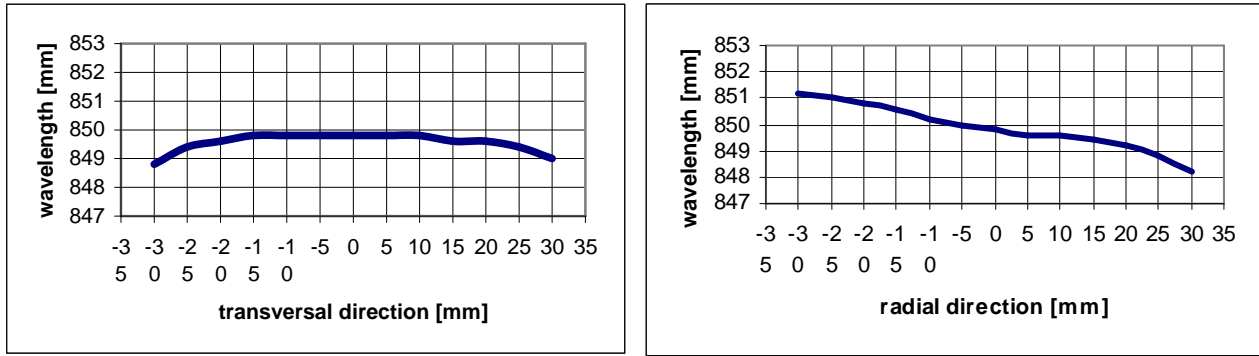


Figure 1: LEFT: Azimuthal cavity resonance variation of MBE grown 850 nm VCSEL structure. RIGHT: Radial cavity resonance variation, increasing numbers indicate larger distance to center axis of the multi wafer MBE system.

The wavelength variation from run to run is depicted in Figure 2 and demonstrates the stability of material flux in the reactor. For 20 runs, representing 100 wafers or roughly 3 Mio devices, the wavelength variation is as small as  $\pm 3$  nm.

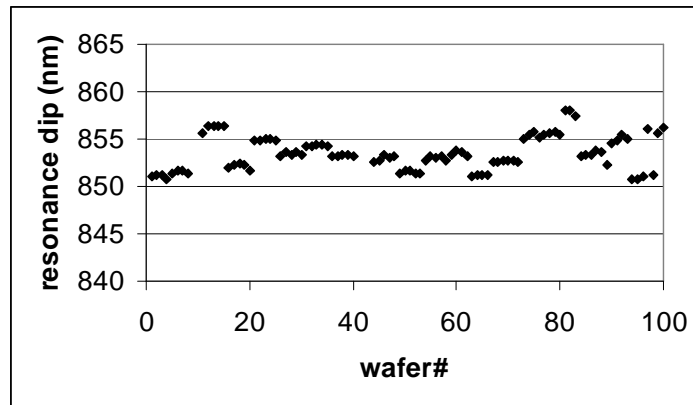


Figure 2: Resonance wavelength dip (center of the wafer) versus epitaxy run. Groups of wafers indicate batches.

Frequently, optical gain and doping profiles are checked on calibration wafers, but most of the feedback to epitaxial growth is derived from quality checks during processing, like spatially resolved reflectance measurements, TLM measurements, and temperature dependent threshold current characteristics.

Compared to standard datacom VCSEL technology, the aperture size of the devices must be controlled extremely well. As a first major requirement the mesa etching that exposes the sidewall of the highly aluminum containing confinement layer must be controlled well in terms of mesa geometries. Precise control of mesa height and mesa diameter is achieved by advanced RIE etching using in-situ control and self aligned hard mask technology. The measurement system shown on the right hand side in Figure 3 takes advantage of laser illumination matched to the DBR stop band and thus provides perfect optical feedback in reflectance mode. On the left hand side in Figure 3 a typical curve of the optical reflectance signal is plotted versus process time. Each DBR mirror pair and the transition from DBR to inner cavity can clearly be recognized and the process can be stopped accordingly after exposing the current confinement layer. Secondly, important parameters for the subsequent oxidation process are process temperature and material composition. Temperature homogeneity across the wafer during the formation of the apertures must be better than  $\pm 0.5$  °C. Ga content of the current blocking layer is much more crucial [8], but can be controlled epitaxially very well. Oxide layer thickness is chosen to be larger than 30 nm although contribution to optical confinement is rather strong, but oxidation rates are much more sensitive on thickness variations for thinner layers [9]. Finally Carbon concentration plays an

important role for the homogeneity of the current confinement layer and needs to be controlled precisely with variations of less than +/- 5 % during the growth of the current confinement layer, too.

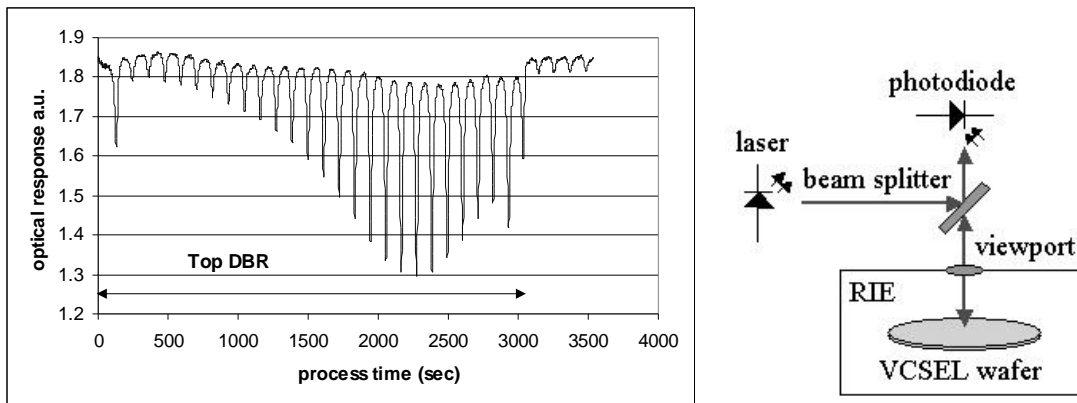


Figure 3: In-situ signal obtained from surface reflection of the processed wafer. The illumination is coupled into the process chamber via beam splitter and viewport.

The challenge is to control all mentioned parameters and thus get very homogeneous oxidation rates across a wafer and from epitaxial run to epitaxial run. Figure 4 depicts the development of aperture size variation with respect to final target along the production runs. In order to optimize yields, the aperture diameter has been tuned by around 0.5  $\mu\text{m}$  along the time line. The data represent more than 2.5 Mio devices.

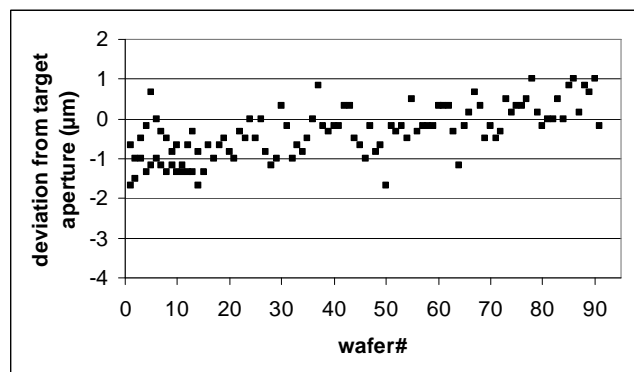


Figure 4: Aperture size monitoring for more than 90 wafers in production. In order to optimize yields, the aperture diameter has been tuned by 0.5  $\mu\text{m}$  during volume production.

By having the described process control available, device yield on wafer can be very high. In chapter "CHARACTERIZATION", yields up to 80 % are reported. In order to reduce cost per piece even further, and of course this is required by high volume consumer applications, the main cost driver needs to be addressed: The footprint of the chip.

Today, typical VCSEL chips are still based on a  $250 \times 250 \mu\text{m}^2$  footprint cell, see Figure 5 (left side). This is mainly due to limitations in dicing and die attach. As a first step scribe and break has been chosen for die separation, since typical dicing streets already consume 25 % of the chip area. In addition U-L-M photonics has established dicing processes that allow for further reduction of the footprint down to  $200 \times 200 \mu\text{m}^2$  (Figure 5 right hand side), which gives a direct increase of parts on wafer by another factor of 1.56. All in all the number of parts on wafer can be increased by almost a factor of 2 compared to standard technology.

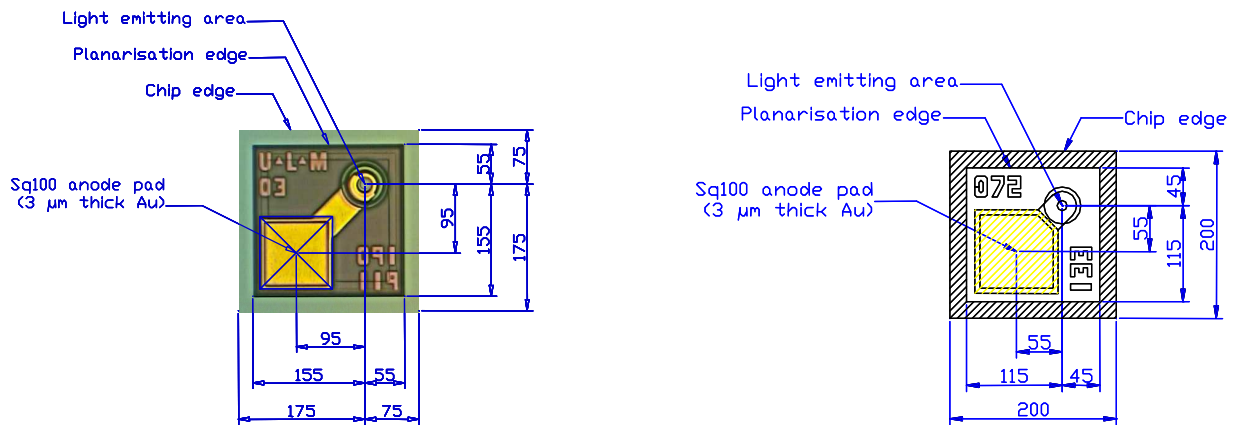


Figure 5: LEFT: standard footprint of a  $250 \times 250 \mu\text{m}^2$  VCSEL unit cell. RIGHT: Reduced footprint to  $200 \times 200 \mu\text{m}^2$ , gaining 56 % increase in number of dice on wafer.

### CHARACTERIZATION

Today, about 55.000 VCSELs are being processed in parallel on one 3-inch wafer. 100 % on-wafer testing is required for quality control, thus highly automated equipment is used to measure all relevant electro-optical parameters like LIV and optical spectra.

Probing of the wafers is done by exact lateral positioning of the individual VCSEL, touching two probes to the bond pad and ramping up the laser current in 100 increments to maximum value of 3 mA. Using the 100 data sets, main laser parameters are derived in real time, like threshold current, slope efficiency, operating voltage, series resistance and many more. The map in Figure 6 illustrates the typical distribution of threshold current.

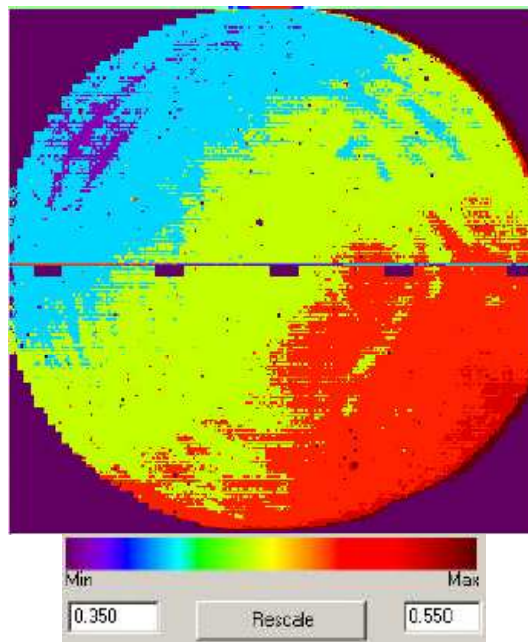


Figure 6: Threshold current distribution on a 3 inch singlemode VCSEL wafer.

Looking at the distribution along the straight line that runs along the diameter of the wafer, the very small variation of only  $\pm 40 \mu\text{A}$  across 3 inch is extracted. In worst case, the span amounts to  $120 \mu\text{A}$ , looking at wafer positions from upper left corner to lower right.

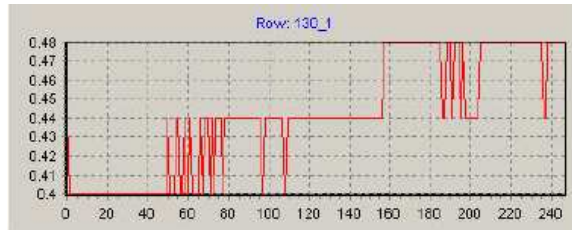


Figure 7: Line scan of threshold current map on wafer diameter.

All devices that pass the LIV parameter selection criteria are then tested on spectral characteristics in a second on wafer mapping sequence. Extracting the required laser current for a certain operation point and the exact position on wafer, high resolution optical spectra of these VCSELs are recorded. The according map of lasing wavelength is given in Figure 8.

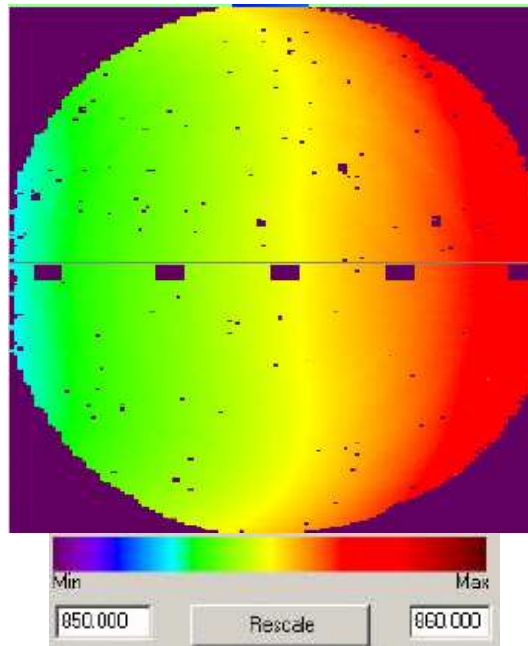


Figure 8: Optical spectra measured on wafer.

In Figure 9 the wavelength variation from 851 nm to 854 nm ( $\pm 1.5$  nm) across the radial growth direction measured at operating current corresponds very well to the measured reflectivity data for epitaxial wafers. Please note the contrary orientation of the gradient, which is only due to axis orientation.

Taking all specifications into account, including LIV performance and spectral requirements, yield on wafer can be as high as 80 %.

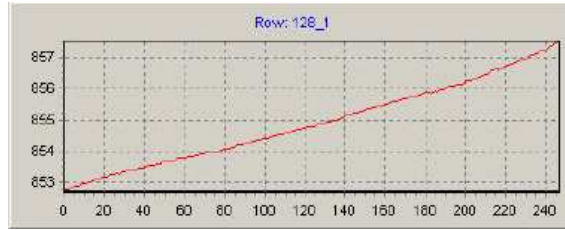


Figure 9: Emission wavelength versus wafer position along the radial growth direction in the MBE reactor.

### LIV, SPECTRAL, AND FARFIELD PERFORMANCE

The LIV characteristics across the 3 inch wafer are very homogeneous as can be seen in Figure 10. Typical values are 0.4 mA threshold current, 0.6 W/A slope efficiency, and 1.5 mA as typical operating current which is given by the eye safety limit of approx. 700  $\mu$ W for 850 nm lasers. Corresponding operating voltages are in the range of 2 to 2.2 V. In the following, the most extreme variation across the wafer along the maximum gradient is depicted. All variations of process parameters like oxide aperture, doping profiles and wavelength variations sum up to only slight variation of threshold current in the order of 100  $\mu$ A and only 150mV operating voltage at 2 mA laser current. The output power at 2 mA laser current ranges between 1.0 and 1.1 mW.

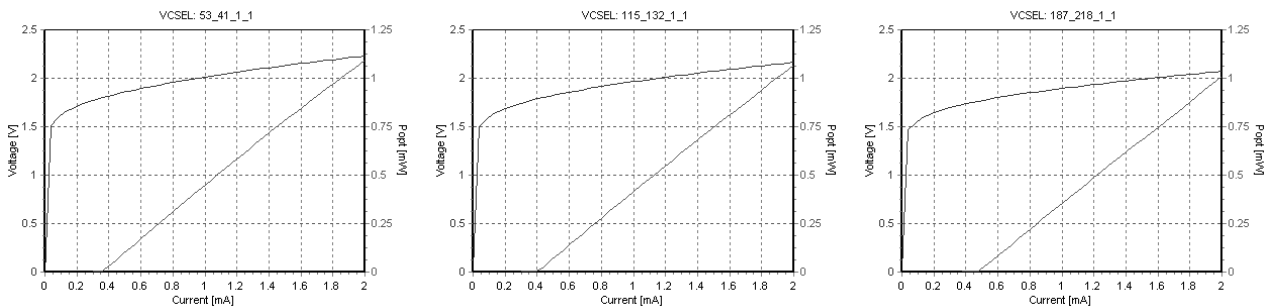


Figure 10: Most extreme variations of LIV characteristics on wafer starting from left to right at top left corner, center of wafer, towards lower right corner.

The LI curves do not show any kinks which indicates that no significant amount of power is transported in higher order modes within the entire current range up to 2 mA.

In Figure 11 the according emission wavelengths at 0.7 mW along the same axis are 856.3 nm, 857.2 nm, and 858.7 nm. All devices show more than 20 dB side-mode-suppression ratio.

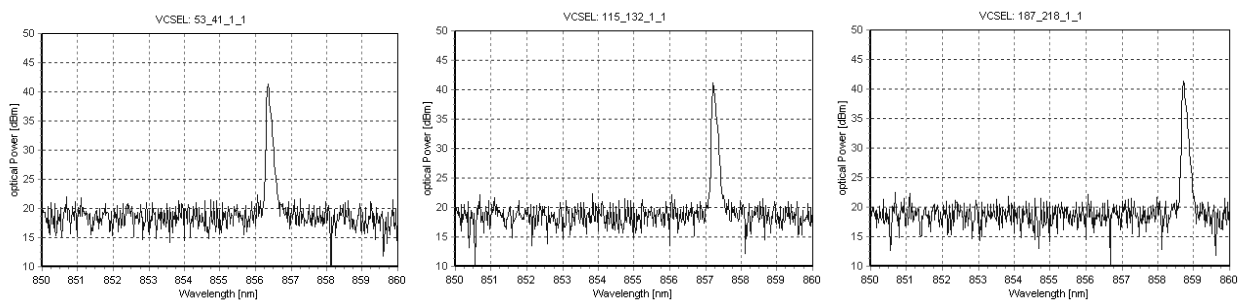


Figure 11: Optical spectra according to LIV characteristics in Fig. 10.

The farfield distribution measured using a pin hole and a photodiode in a 20 cm distance shows nice gaussian singlemode characteristics as can be seen in Figure 12. The beam divergence typically amounts to 12° FWHM and is pre-defined by the small size of the current aperture and the strong wave guiding.

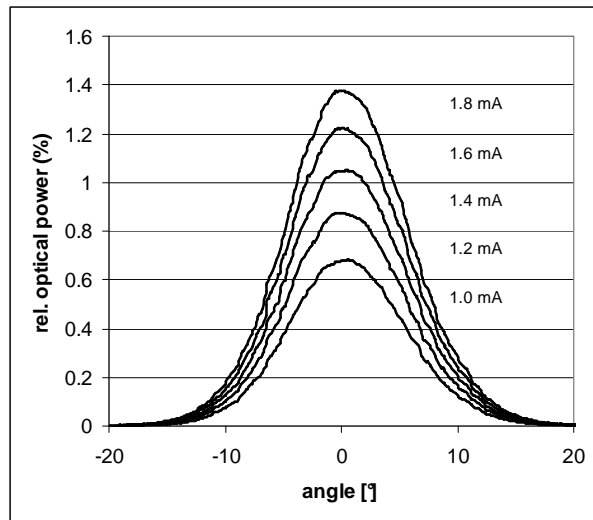


Figure 12: Farfield characteristics of a singlemode VCSEL at various laser currents.

### PACKAGING

For low cost packaging the devices can be either packaged in surface mount type packages or TO type packages. Figure 13 shows two typical packages used at U-L-M photonics for VCSEL packaging. On the left hand side, we can see the standard TO 46 package with flat window cap. On the right hand side we can see a 1206 SMT type package having an ceramic carrier and an epoxy encapsulation.

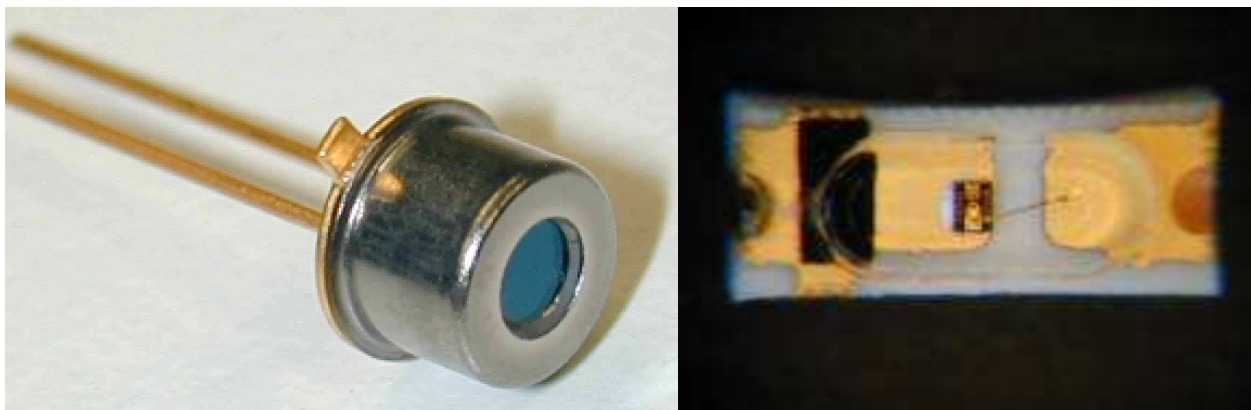


Figure 13: TO 46 can and size 1206 surface mount type package.

TO type packaging for VCSELs is a very mature technology, which is used since many years in single channel datacom applications. It has the further advantage, that the package can be hermetically sealed, with the disadvantage of higher cost of this package type. SMD type packages have typically a lead frame or ceramic carrier for the chip and an epoxy encapsulation. The technology of LED packaging can directly be adapted to be used for the VCSEL. During packaging very stringent ESD protection of the devices is necessary. Packaging of the devices together with an ESD protection diode gives increased ESD damage thresholds of the packaged devices compared to the VCSEL chip. Typical ESD damaged thresholds of the unprotected die are in the range of 70 V according to the human body model (HBM). Whereas by using ESD protection diodes, ESD damage voltages in excess of 2 kV can be achieved.

After packaging of the device together with the ESD protection diode, a burn-in and final test is conducted. The burn-in can help to screen out devices, which show infant mortality. More details about this can be found in the next section.

## RELIABILITY

Typical applications in consumer products require a lifetime of up to 50 000 hours with better than 100 ppm failed devices during this period. Operation conditions are 0 to 50 °C ambient temperature and up to 85 % relative humidity. The very high susceptibility of singlemode VCSELs to ESD is a further challenge.

Since the production and packaging of singlemode VCSELs in very high volumes was a new task for U-L-M photonics, a very extensive qualification of the devices has been conducted. **Table 1** gives an overview of the different tests. The tested devices were picked from 3 different production lots.

Table 1: Different tests conducted during qualification of TO can packaged 850 nm singlemode VCSELs.

Test type:	Number of tested devices:	Test conditions:	Failure criteria:
Low temperature storage	3x45	-40°C, 1000h	+10%/-25% change in optical power
High temperature storage	3x45	85°C, 1000h	+10%/-25% change in optical power
Low temperature operation	3x45	-40°C, 1000h	+10%/-25% change in optical power
High temperature operation	3x800	80°C, 100°C, 1000h	+10%/-25% change in optical power
Temperature cycling	3x45	40°C to +85°C, 40°C/minute, 500cycles	+10%/-25% change in optical power
Temperature humidity bias	3x80	85°C/ 85%RH, 500h	+10%/-25% change in optical power
High current life	3x30	170°C, 3mA	+10%/-25% change in optical power
Aging life	3x60	140°C, 170°C, 2mA, 300h	+10%/-25% change in optical power
Solder heat resistance	3x10	260°C ± 5°C for 10s	+10%/-25% change in optical power
Solderability	3x5	JESD22-B102	+10%/-25% change in optical power
Chemical sensitivity	3x5	Isopropyl Alcohol and Solder flux	+10%/-25% change in optical power
Vibration	3x10	20G 20-2000 Hz	+10%/-25% change in optical power
ESD	3x30	2kV HBM, 0.5kV CDM, 0.2kV MM	+10%/-25% change in optical power

The lifecycle of a product is typically divided into three lifetime regimes. The first regime is called the Early Failure Period or Infant Mortality Period, which is often subject to higher failure rates. This period is followed by the intrinsic failure period which shows often a constant but low failure rate. Due to the very low failure rates during this period, it is very difficult to get any values. At the end of the lifecycle of the product, the failure rate increases again. This period is called the Wearout Failure Period. In the following subsections, we want have a closer look into these different lifetime regimes.

### Infant failures:

During the infant failure regime, the failure rate can be high due to devices with defects that allows them to be within specification but show very fast degradation and leading to early failure of the device. Typical defects can be dislocations in the epitaxial layers or electrostatic induced defects. To sort out these devices a burn-in can be conducted. During burn-in the devices are operated at accelerated conditions for a certain period of time. After this burn-in the devices are measured again and the devices which failed are sorted out. **Table 2** shows how many devices failed during a 16 h burn-in at 100 °C ambient temperature. Based on this number we get a failure rate of approximately 200ppm.

Table 2: Four production batches with number of devices failing during 16h burn-in @ 100°C ambient temperature and 3mA bias current.

Batch	Total	Failures	Failures (%)	Failures (ppm)
B050620B	4240	1	0.0236	235.8491
B050708F	5640	1	0.0177	177.3050
B050710C	7460	1	0.0134	134.0483
B050705A	8520	3	0.0352	352.1127
	<b>25860</b>	<b>6</b>	<b>0.0232</b>	<b>232.0186</b>

**Spontaneous failures:**

The most difficult task during qualification phase was to get values for the spontaneous failure rate. Less than 100 ppm failures in the first 50 000 hours of operation corresponds to a failure rate better than two failures in one billion hours of operation. In normal use conditions this would translate into testing of more than 100 000 VCSEL for one year with having afterwards 2 failures. Since this is not possible, we decided to stress the devices harder than in normal use conditions. **Table 3** gives an overview on the tested batches. As stress parameter we used the ambient temperature, which was set at 80 °C and 100 °C. Assuming an activation energy of 0.7 eV we get an acceleration factor of 25 and 80 respectively. We assumed a normal use condition of 1.5 mA bias current and 40 °C ambient temperature. The cumulated testing time at normal use conditions correspond now to more than 200 million test hours with only 2 failed devices.

Table 3: Conditions for high temperature operation life test during qualification phase.

Batch#	Number of devices	Operation conditions	Test time (h)	Acceleration factor to normal operation (40°C, 1.5mA) (0.7eV)	Test time @ normal operation conditions (h)	Total test hours	# of failures	Failures rate (FIT)
B050408A	800	2mA, 80°C	2200	25	55000	44 000 000	0	0
B050408B	800	2mA, 100°C	2600	80	208000	166 400 000	2	12
B050620B	800	2mA, 80°C	600	25	15000	12 000 000	0	0
					Total:	222 400 000	2	9

Figure 14 shows the operation current for 0.5mW output power for 2200 hours of operation at 2 mA bias and 80 °C ambient temperature. The diagram shows the data of one test board with 40 VCSELs.

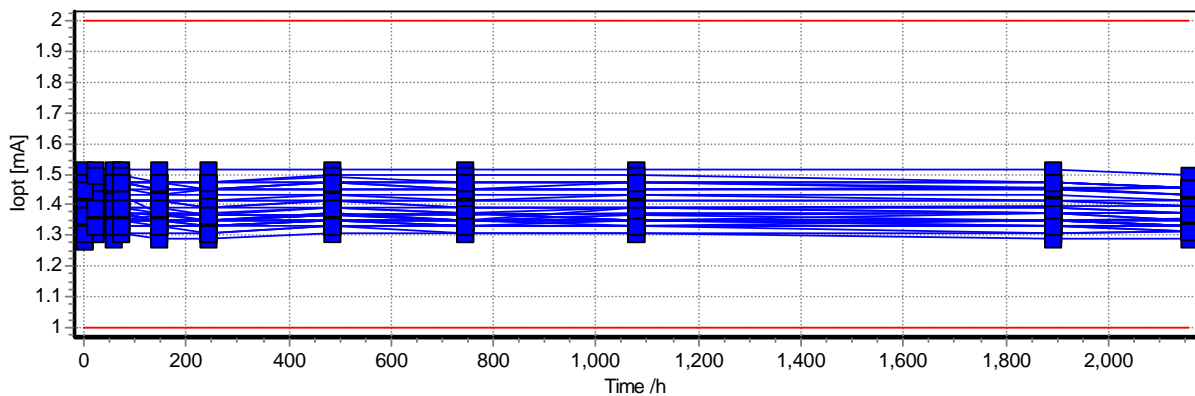


Figure 14: VCSEL operating current for 0.5mW output power of 40 VCSEL subject to high temperature operating life.

**Wear out failures:**

In order to get values for the wear out behavior of the devices, different tests at highly accelerated conditions have been conducted. The tests were conducted on chip level using special reliability boards, since standard test boards can not withstand the high ambient temperatures of up to 170 °C.

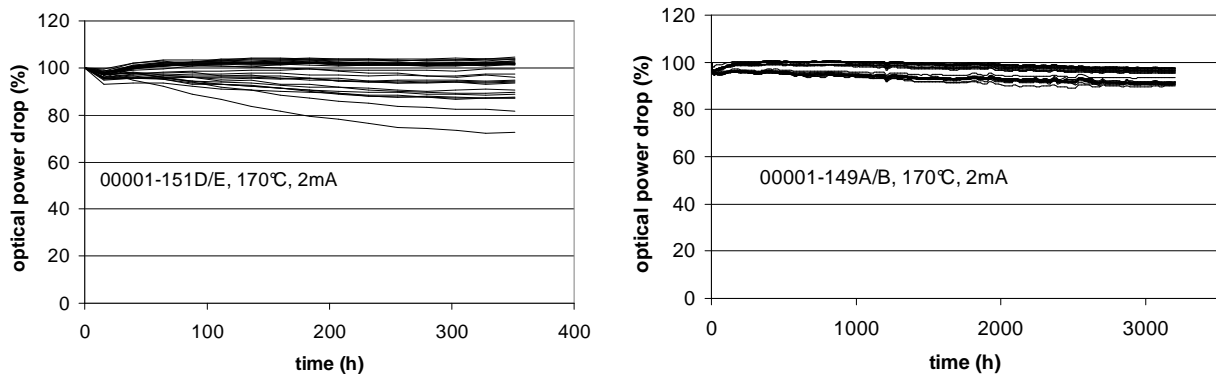


Figure 15: Relative optical power drop during high temperature operation life test of chips from different processing lots and 2 different epitaxial growth runs.

Figure 15 shows the relative optical power drop of 60 devices on two test boards, representing 4 processing batches and 2 epitaxial growth runs. Both test boards do not show failures for the first 350 hours and 3000 hours respectively. Anyway, the two different growth runs show a clear difference in behavior during highly accelerated life testing (HTOL). The devices from growth run 00001-151 show much stronger change in optical power during HTOL than devices from growth run 00001-149. The reason for the different behavior is not yet clear. One explanation might be a difference in thermal impedance, which depends strongly on active diameter.

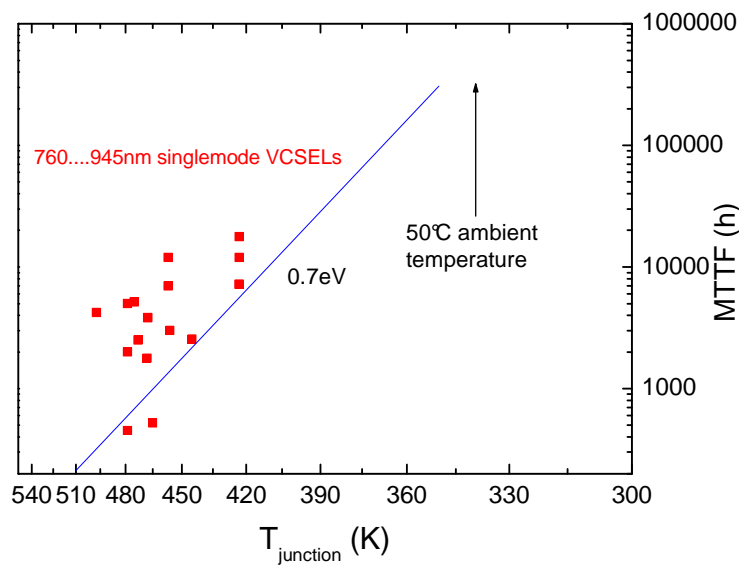


Figure 16: Arrhenius plot of MTTF values versus junction temperature for different types of singlemode VCSELs. We have included in the plot a line for 0.7eV activation energy.

In order to be able to predict when wear out phase is starting, some batches were operated in HTOL until at least 50 % of the devices showed a power drop of more than 2 dB. The time when 2 dB power drop is reached, is defined as time to failure (TTF). By fitting the TTF values to a lognormal distribution, values for the mean time to failure (MTTF) and

distribution parameter sigma can be extracted. Figure 16 shows the Arrhenius plot for singlemode VCSELs of different emission wavelength. Each point represents the MTTF value of an ensemble of 15 to 30 devices tested at the same operation conditions. The line gives the acceleration for 0.7 eV activation energy. The plot clearly shows, that the wear out phase is well above the requested 50 000 h for normal operation conditions around 25 °C.

### Ongoing reliability tests:

In semiconductor laser production it is very essential to do ongoing reliability testing in order to find any problems related to epitaxial growth or packaging. Especially the very high susceptibility of the singlemode VCSELs to electrostatic discharge makes ongoing monitoring of the production line necessary. **Table 4** gives an overview on typical tests conducted on the finished product.

Table 4: Example for ongoing reliability testing for 850nm singlemode VCSEL chip production.

Test	Test Conditions	Test Frequency
Light Current Voltage Characteristics over Temperature	-10...85 °C	3 pcs every epitaxial batch
Farfield Profile	0.5...2 mA, 25 °C	3 pcs every epitaxial batch
High Temperature Operation (HTOL)	>150 °C, > 2 mA	15 pcs every wafer
Temperature Humidity Bias	85 °C/85 % RH, 1.5 mA	15 pcs every wafer
Light Current Voltage (LIV) Characteristics	Room temperature	Every device
Spectral Characteristics	Room temperature	Every device
Temperature Humidity bias (THB)	85 % r.h., 8 5°C, 1.5 mA	10 devices /week

Since we are doing LIV testing before and after burn-in of the packaged devices, we have access to statistical data on early failures and packaging yield and any problems linked to high infant mortality or spontaneous failure rate can be detected prior to delivery to the customer.

## APPLICATIONS

The first application that requires high volume fabrication of singlemode VCSELs is position tracking in PC mice. The optical engine requires a coherent laser source that enables high definition surface tracking, independent on kind of surface. The very low power consumption of less than 2.5 mW is very advantageous for battery driven devices like wireless desktop equipment.

Additional applications are foreseen in high definition optical encoders and rotary position transducers.

In future, also spectroscopic applications like tunable diode laser absorption spectroscopy or optical pumping of frequency normals will show growing demand in oxygen gas sensing and atomic clock applications (GPS receivers or clock distribution in telecom networks).

## SUMMARY

In this paper we describe advanced manufacturing techniques that enable low cost production of oxide confined single-mode VCSELs for high volume applications. Epitaxial growth and processing techniques are reviewed that allow manufacturing of wafers with very high homogeneity of device parameters. The extensive qualification procedure is discussed in detail, showing that the reliability of these singlemode VCSEL is comparable to multimode VCSELs.

Further research and development in manufacturing of singlemode VCSELs will mainly investigate advanced packaging technology and further integration of the devices on system level.

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